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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	13

DATE MAILED: 12/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/478,714	Applicant(s) EL-KIK ET AL.	
	Examiner David J. Huisman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1, 3-11, and 14-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment "C" as received on 11/13/2003.

Amendment Format Comments

3. It is not clear to the examiner why there are breaks in the underlining of added claim limitations. For instance, why is there a break in underlining between "and" and "the" in claim 7, and "the" and "second" in claim 7? Also, why has the applicant deleted spaces? For instance, in claim 10, in the 3rd paragraph, the applicant has removed the space between "second" and "one". Likewise, in claim 14, the applicant has deleted the space between "processors" and "is". Finally, more breaks in underlining exist in claim 15. In addition, without underlining, deletion of a space by strikeout and insertion of a hyphen are indistinguishable and so it's also not clear whether the applicant wanted to delete the space (thereby creating spelling errors due to the combination of words that should not be combined) or insert a hyphen (thereby crating grammatical errors).

Claim Objections

4. Claims 4 and 5 are objected to because of the following informalities: Please replace "and a least one second processor" with --and at least one second processor-- . Appropriate correction is required.

5. Claims 9 and 16 are objected to because of the following informalities: The examiner recommends removing "and" from the phrase "and a memory bank field". Appropriate correction is required.

6. Claims 9 and 16 are objected to because of the following informalities: It is not clear how the control word comprises a computer readable medium since a control word is a piece of data. Data does not comprise of a computer readable medium. Instead, data would be stored on a computer readable medium. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 4 and 5 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a dual processor system (a main processor and a co-processor), does not reasonably provide enablement for "a first processor and at least one second processor," i.e., there is no enablement for having more than one coprocessor (a third or fourth coprocessor). The specification does not enable any person skilled in the art to which it pertains,

or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

9. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a dual processor system (a main processor and a co-processor), does not reasonably provide enablement for "a system having many selectable devices such as other co-processors," i.e., there is no enablement for having more than one coprocessor. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1, 3-11, and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Campanini, U.S. Patent No. 4,700,292 (as applied in the previous Office Action and herein referred to as Campanini).

12. Referring to claim 1, Campanini has taught a dual processor system, comprising:

a) a first processor coupled to a system address bus and a data bus. See Fig.1 and note that a first processor EL_A is coupled to a bus BC, which is used to transmit both data and addresses to a second processor EL_B. For instance, during burst transfer, both a starting address is passed along

BC to the second processor (making it an address bus in that it passes addresses) and the actual data to be transferred will eventually follow (making a data bus in that it passes data).

b) a second processor coupled to the system address bus and to the data bus (See Fig.1, component EL_B), the second processor comprising:

b1) a control register having a control register system address. Note the control register comprises the MEA and WCA storage locations in Fig.5. Both of these locations control the second processor during transfer mode. Also, note that these registers are read from and written to for increment and decrement purposes, respectively (see column 9, lines 27-34). Therefore, in order to read and write to specific locations, the control registers must be addressable.

b2) an internal memory. See fig.1, components DIS_B and MED_B.

b3) a data register having a data register system address and coupled to the internal memory. See Fig.4, and note the REI register. This data register receives all incoming words where the words are then propagated to the buffer store (FIFO) and ultimately, to the appropriate destination within the internal memory. Also, note that the WR signal, which indicates a write is going to occur, is used to specify a word is being transferred. See column 9, lines 27-34. Therefore, the WR signal will act as a system address for the data register in that it results in the data register receiving some data. Note also that this data register is coupled to the internal memory since the internal memory is the final destination for the transferred words.

b4) and an internal address generator coupled to the control register and to the internal memory. See column 9, lines 26-34. Note that the MEA control register initially holds

the starting internal memory address. This address is incremented by an internal address generator each time a new word is being transferred to memory.

c) a control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus. Note that header data is sent prior to the actual data words that are to be transferred. See the abstract. This header includes the number of words to be transferred and the starting destination address. See column 2, lines 33-38, and column 8, line 61, to column 9, line 10. Note that the control register is addressed appropriately, such that the word count is put in the WCA control register and the starting address is put in the MEA register. Addresses need to be provided in order to select one of these registers.

d) the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode. See column 9, lines 24-38. Note that the word count, stored in the WCA register, includes a burst mode indication. If the word count is stored as an X-bit number, then the X-1 most significant bits are the burst mode indicators. If any one of those bits is set to 1, then that bit is a burst mode bit. This can be seen with a simple example. Suppose, one word is to be transferred (non-burst mode) and the word count is appropriately set to 00000001 (where X=8). The seven (X-1) most significant bits are set to 0, indicating that the processors are not in burst transfer mode. However, if three words were to be transferred and the word count were set to 00000011, then it can be seen that

one of the seven most significant bits is set to 1, indicating burst mode. Therefore, that bit would be a burst mode bit.

e) in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations. See column 9, lines 24-38. Basically, the first processor asserts the WR signal, specifying a write to the data register and then transfers the data word to be written. This word will then be stored at the address specified by the MEA register, where the value of this register is incremented for as many words that are to be transferred, which is specified by the WCA register.

f) in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor. See column 9, lines 24-38, and column 1, lines 7-10, and note that the relationship between processors is interchangeable, i.e., the first processor can be the sender or the receiver. In this situation, when the first processor is to receive from the slave, this would be read mode, and it would work much like the write mode mentioned above.

13. Referring to claim 3, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus. From column 9, lines 24-38, the WR signal is asserted just before each incoming word arrives via bus BC and is stored in the data register (REI). As long as the data register system address signal WR is applied, then data still needs to be transferred. Once there is no data left to transfer, the WR signal will not be applied, and burst mode will be finished. If the WR signal is no longer asserted, then clearly no more incoming data is arriving.

14. Referring to claim 4, it has been noted by the examiner that claim 1 includes all limitations claimed in claim 4. Therefore, claim 4 is rejected for the same reasons set forth in the rejection of claim 1 above. In addition, Campanini has taught many selectable devices such as other coprocessors (see Fig. 1, note that different memories may be selected as well as a coprocessor), a data bus (see Fig. 1, component BC), a chip select line (see Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55), a read signal line (see Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44), and a write signal line (see Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation).

15. Referring to claim 5, it has been noted by the examiner that claim 1 includes all limitations claimed in claim 5. Therefore, claim 5 is rejected for the same reasons set forth in the rejection of claim 1 above. In addition, Campanini has taught many selectable devices such as other coprocessors (see Fig. 1, note that different memories may be selected as well as a

coprocessor), a data bus (see Fig.1, component BC), a chip select line (see Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55), a read signal line (see Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44), and a write signal line (see Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation).

16. Referring to claim 6, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor is a co-processor. See column 1, lines 29-43 and note that the second processor (slave) will assist the main processor if the main processor malfunctions or even if it doesn't malfunction (as described in column 3, lines 26-28).

17. Referring to claim 7, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, and the data is transferred from the first processor to a specified location into memory of the second processor during a next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode. As described in the rejection of claim 1(d) above, when the number of words to be transferred is 00000001 (assuming the word count register WCA holds an 8-bit value), the seven most significant bits do not indicate burst mode. Therefore, the second processor will enter a single data transfer mode, which would correspond with the value 1 in the WCA register.

18. Referring to claim 8, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught that the first processor and second processor are intercoupled by

a) the system address bus and the data bus to select a co-processor in a system having many selectable devices such as other co-processors. Recall from the rejection of claim 1 that the BC bus shown in Fig.1 is a system data/address bus. Also, note from Fig.1, that multiple devices, such as mass memory, working memory, and interface chip, and coprocessor.

b) a chip select line. See Fig.2 and note the AK signal. This signal results in the activation (selection) of the REI chip. See column 6, lines 47-55.

c) a read signal line. See Fig.2 and note the RY signal, which signifies that the second processor is ready to read transferred data. See column 6, lines 39-44.

d) a write signal line. See Fig.2 and column 9, lines 24-38 and note that the WR signal is used to signify a write operation.

19. Referring to claim 9, Campanini has taught a dual processor system as described in claim 1. Campanini has further taught:

a) the internal memory comprises a computer readable medium having a plurality of memory blocks wherein data are stored in consecutive locations. A memory is inherently computer readable. The internal memory has multiple addressable locations so each location can be considered a block of memory where data can be stored. Data will also be stored in consecutive locations by incrementing the contents of the MEA register (which is loaded with the starting address)

b) the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank. Again, recall the header (control word) data described in the rejection of claim 1 above. This control

word contains multiple fields, where the data held in these fields is put into control registers MEA and WCA. The burst mode bit field would be the field holding the X-1 most significant bits of an X-bit word count (which is placed in the WCA register). Any one of these bits, when set, would indicate burst mode transfer. Note also that there are two banks of memory: one is referred to as the working memory, while the other is the mass memory (see Fig.1). According to the abstract, the data is first transferred to the second processor's working memory and from there it is transferred to the main memory. Therefore, the word in the MEA register can be considered both a memory bank field and an internal address bank field. This address specifies the starting memory destination address (which is incremented during burst mode). However, this word can also be interpreted as a memory bank field in that the address represents an address of the working memory, thereby implicitly selecting the working memory as opposed to selecting the mass memory.

20. Referring to claim 10, it has been noted by the examiner that the only difference between claim 1 and claim 10 is that claim 1 claims a multiprocessor system comprising a plurality of interconnected processors each having internal memory. However, Campanini has taught a multiprocessor system (Fig.1) with a plurality of interconnected processors (Fig.1) each having internal memory (Fig.1, components DIS and MED). Furthermore, claim 10 is rejected for the same reasons set forth in the rejection of claim 1.

21. Referring to claim 11, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 3 and claim 11 is that claim 3 claims a dual processor system while claim 11 claims a multiprocessor

system. However, a dual-processor system is a multi-processor system. Consequently, claim 11 is rejected for the same reasons set forth in the rejection of claim 3.

22. Referring to claim 14, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 6 and claim 14 is that claim 6 claims a dual processor system while claim 14 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 14 is rejected for the same reasons set forth in the rejection of claim 6.

23. Referring to claim 15, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 8 and claim 15 is that claim 8 claims a dual processor system while claim 15 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 15 is rejected for the same reasons set forth in the rejection of claim 8.

24. Referring to claim 16, Campanini has taught an integrated circuit as described in claim 10. Furthermore, it has been noted by the examiner that the only difference between claim 9 and claim 16 is that claim 9 claims a dual processor system while claim 16 claims a multiprocessor system. However, a dual-processor system is a multi-processor system. Consequently, claim 16 is rejected for the same reasons set forth in the rejection of claim 9.

Response to Arguments

25. Applicant's arguments filed on November 13, 2003, have been fully considered but they are not persuasive.

26. In the remarks, Applicant argues the novelty/rejection of claim 1 on pages 8-9 of the remarks, in substance that:

> "the present invention has no component that provides for a decrementation of the numerical value stored within a word counter. Conversely, Campanini neither discloses nor suggests: a control register that does not contain any word count, but nonetheless achieves the transfer of data from one memory to another."

27. These arguments are not found persuasive for the following reasons:

a) It should be realized that applicant has made use of the term "comprising" within claim 1. And,

> "The term comprises is inclusive and fails to exclude unrecited steps. In re Horvitz, 168 F 2d 522, 78 U.S.P.Q. 79 (C.C.P.A. 1948). The use of the term comprising to introduce the claimed structure means that the device covered by these claims may involve many more elements than those positively recited. Ex parte Gottzein et al., 168 U.S.P.Q. 176 (PTO Bd. App. 1969). Comprising leaves the claim open for the inclusion of unspecified ingredients even in major amounts. Ex parte Davis et al., 80 U.S.P.Q. 448 (PTO Bd. App. 1948)."

As a result, Campanini still reads on claim 1 even though it uses a counter value. The applicant has never explicitly excluded this counter component, and the term "comprising" within the claim allows extra steps (or components) to exist within the prior art.

28. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 9 of the remarks, in substance that:

> "The MEA [in Campanini] represents an address register that is loaded with the address of the cells of the working memory. The current invention, by contrast, begins with a pointer and increments the pointer every time there is an access by the coprocessor. A pointer increments from a base point, but is not an address in and of itself."

29. These arguments are not found persuasive for the following reasons:

a) It is not clear what the applicant is arguing. First of all, a pointer is an address and this is supported by the Free On-Line Dictionary of Computing's definition of "pointer," which has been provided for applicant. Secondly, it is not clear as to why the applicant believes that Campanini is different from the present invention. Starting addresses are supplied in both inventions and both are incremented during burst transfer.

30. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 9 of the remarks, in substance that:

> "...(the present disclosure utilizes no code correction) and the present invention control register does not decrement any count. Additionally, the data register [of the present invention] does not store the number of words to be transferred and does not decrement any number thereafter, but receives a word of data..."

31. These arguments are not found persuasive for the following reasons:

a) As explained above in paragraph 11, the applicant has not excluded such features from the present invention. Therefore, if the present invention claims feature "A," and Campanini has taught features "A," "B," and "C," then Campanini still reads on the claims. In addition, it should be realized that the word count is stored in the WCA and not the REI. Instead, the REI is the receiving point for all data which comes in over bus BC, as shown in Fig.4 of Campanini. Looking at this figure, it should be seen that once the data travels along bus BC to the coprocessor, it can only go to the Outgoing word register or incoming word register. Clearly, the data is incoming, so it will be put in the incoming word register. From there, the word count would be ultimately sent to the WCA, just as the data that has arrived at the REI will ultimately be stored in memory during burst transfer.

32. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 10 of the remarks, in substance that:

> "Firstly, characterizing the REI, MEA, or WCA as data registers is inappropriate in that they are counters."

33. These arguments are not found persuasive for the following reasons:

a) The examiner has been unable to locate any portion of Campanini that states that all three of these registers are counters. The WCA register may be considered a counter in that it counts how many words are left to be transferred during the burst operation. However, the MEA register holds an address which is updated during the burst transfer to point to consecutive memory locations. Finally, the REI receives all of the data that is sent to the coprocessor, which should be realized since the REI is the incoming word register, i.e., all incoming data is sent there. Secondly, a "data register" is nothing more than a register which holds some type of data. Even a counter, such as WCA, still holds data, where the data comprises binary digits representing a current count value.

34. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 11 of the remarks, in substance that:

> "The only relation to the control register [by Campanini] is that it does contain an address, but not an address to be decremented. WCA and MEA have no functional relation to the control register in the present invention."

35. These arguments are not found persuasive for the following reasons:

a) In applicant's claim 1, the control register stores a control word having a burst mode bit and a starting internal address. Campanini's WCA and MEA do the exact same thing in that an internal address is stored in the MEA and the count in WCA will include a burst mode bit, i.e. as

long as at least one of the seven most significant bits in the WCA is set to 1, burst mode will occur. Applicant does not exclude decrementing any counter within the claims.

36. In the remarks, Applicant argues the novelty/rejection of claim 1 on page 11 of the remarks, in substance that:

> "The examiner thus finds a burst mode in Campanini, where such does not exist. The inventors have chosen to define burst mode as incrementing the address without decrementing the word count..."

37. These arguments are not found persuasive for the following reasons:

a) As described above, the claims include no language regarding the exclusion of decrementing a word count. Clearly Campanini does teach a burst mode in that a starting address is provided, and data will be stored at consecutive storage locations, starting at the starting address, by incrementing the starting address each time new data is to be stored. The examiner is unclear as to how Campanini's burst mode differs from the burst mode in the present invention.

38. In the remarks, Applicant argues the novelty/rejection of claim 3 on page 12 of the remarks, in substance that:

> "Campanini neither discloses nor suggests that when processor 110 wishes to end the burst data transfer, it may, for example, assert the system address of some other control register, or of control register 121 and write all 0s into the control register. In fact, only when there is no data left to transfer does the WR signal stop being asserted."

39. These arguments are not found persuasive for the following reasons:

a) The applicant is arguing something which does not exist within claim 3. Nowhere in claim 3 does it mention that burst mode can be stopped by asserting the system address of another register or writing all 0s into the control register. In general, claim 3 only mentions that burst

mode will continue as long as the data register address is asserted. In Campanini, burst mode will only continue as long as the WR signal is asserted. The WR signal acts as a data register address since every time it is asserted, it signifies that new arriving data will be stored in the REI which will be written during burst mode (see column 9, lines 27-30...note that WR is asserted before each incoming word arrives).

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
December 18, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER